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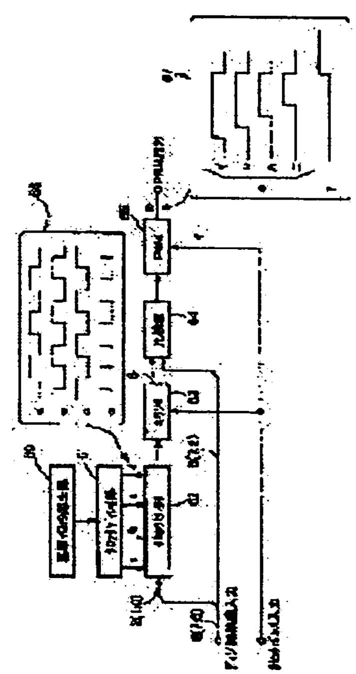
(54) PICTURE DISPLAY DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a picture display device in which a good quality picture having a high gradation is obtained without increasing the frequency of a PWM clock even though the PWM interval becomes shorter as the frequency of horizontal scanning becomes higher.
SOLUTION: A clock delay section 61 generates four kinds of clocks having different phases from a reference clock generated by a reference clock generating section 60 and a clock selector 62 selects one clock from among the four kinds of clocks in accordance with the low-order bit of digital video signals. A counter 63 counts the selected clock and its output and the high-order bit of the digital video signals are compared in a comparator 64. A PWM section 65 determines the rising position of the output waveforms based on the result of the comparision. The falling position is determined according to a reset pulse input and fixed.



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CLAIMS

[Claim(s)]
[Claim 1] It is the image display device which performs a gradation display by the Pulse Density Modulation to which the width of face of the pulse for a display in each period which divides the horizontal scanning period of a video signal and is acquired is changed according to the magnitude of a video signal. A means to generate two or more clocks with which phases differ, and a clock selection means to choose one clock from said two or more clocks according to a video-signal input, The image display device equipped with a means to change the standup location of a Pulse-Density-Modulation output signal, based on the selected clock.
[Claim 2] Said clock selection means chooses one clock from said two or more clocks according to the lower bit of a digital video-signal input. The counter with which a means to change the standup location of said Pulse-Density-Modulation output signal counts said selected clock, The image display device containing the comparator which compares the high order bit of the output of said counter, and said digital video-signal input, and the PWM section which determines the standup location of a Pulse-Density-Modulation output signal based on the output of said comparator according to claim 1.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the image display device which performs a gradation display by Pulse Density Modulation (PWM:Pulse Width Modulation).
[0002]
[Description of the Prior Art] The conventional example of this kind of image display device is shown in drawing 2 . Drawing 2 is the decomposition perspective view mainly showing electrode structure. The cathode 2, the electron beam drawer electrode 3, the signal modulating electrode 4, the focusing electrode 5, the horizontal deflection electrode 6, the vertical deflection electrode 7, and screen 8 as a back plate 1 and a source of an electron beam are arranged in order toward the front (drawing Nakamigi side) from back (left-hand side in drawing), these components are contained inside a vacuum housing (illustration abbreviation), and this image display device is constituted.
[0003] The cathode 2 as a source of an electron beam is horizontally stretched so that the electron beam horizontally distributed over a line can be generated, and this cathode 2 keeps predetermined spacing perpendicularly, and is formed in it two or more. In drawing 2 , although only seven of 2I-2TO are shown since it is easy, 28 cathodes 2I-2Ma are arranged at intervals of 3mm in fact. Large spacing of a cathode cannot be taken freely but is regulated by spacing of the vertical deflection electrode 7 and a screen 8. As a cathode 2, what applied the oxide-coated-cathode ingredient to the front face of a tungsten rod with a diameter of 10-30 micrometers is used. And a cathode 2 is controlled so that upper cathode 2 I to cathode 2 downward Ma emits a fixed time amount [every] electron beam in order.
[0004] A back plate 1 has the function which extrudes an electron beam only in the direction of an anode while inhibiting generating of the electron beam from line cathode other than the line cathode under drive. In drawing 2 , although the vacuum housing is not shown, it can also be made into the structure where a back plate 1 serves as the tooth back of a vacuum housing.
[0005] The electron beam drawer electrode 3 counters with each of cathodes 2I-2Ma, and consists of an electric conduction plate 11 which has two or more through tubes 10 which kept predetermined spacing and were put in order horizontally, and the electron beam emitted from the cathode 2 is taken out through a through tube 10.
[0006] It consists of a long electric conduction plate 15, and this electric conduction plate 15 keeps predetermined spacing in perpendicularly the signal modulating electrode 4 has a through tube 14 with each of cathodes 2I-2Ma in the location where it counters, and is horizontally installed in it side by side. [two or more] In drawing 2 , although only eight electric conduction plates 15 for signal modulating electrodes are shown since it is easy, 114 electric conduction plates 15 for signal modulating electrodes are arranged in fact. The signal modulating electrode 4 is synchronized with the timing of the horizontal deflection which moreover mentions later each through put of the electron beam classified horizontally corresponding to the picture element of a video signal, and is controlled by the electron beam drawer electrode 3.
[0007] A focusing electrode 5 consists of an electric conduction plate 17 which has a through tube 16 in each through tube 14 prepared in the signal modulating electrode 4, and the location

which counters, and serves to converge an electron beam. A horizontal deflection electrode 6 consists of an electric conduction plate 18 of the pair perpendicularly prolonged along with the horizontal both sides of the lengthwise direction list of the through tube 16 formed in the electric conduction plate 17, and 18', and the electrical potential difference for horizontal deflection is impressed to each electric conduction plate. Thereby, the electron beam for every picture element is deflected horizontally, respectively, carries out a sequential exposure and makes each fluorescent substance of R, G, and B emit light on a screen 8. In this configuration, an electron beam is horizontally deflected by two trios.
[0008] The vertical deflection electrode 7 consists of an electric conduction plate 19 of the pair which is arranged in the perpendicular direction mid-position of the through tube 16 formed in the electric conduction plate 17 as a focusing electrode 5, and is prolonged horizontally, and 19', and the electrical potential difference for vertical deflection is impressed to each electric conduction plate. Thereby, an electron beam is deflected perpendicularly. In this configuration, the electron beam produced from one cathode is perpendicularly deflected by eight lines. And with the vertical deflection electrode 7 of 29 sheets, 28 pairs of vertical deflection conductor pairs corresponding to each of 28 cathodes 2I-2Ma are constituted, and, thereby, 224 horizontal scanning Rhine is perpendicularly drawn on a screen 8.
[0009] In this configuration, the horizontal deflection electrode 6 and the vertical deflection electrode 7 are arranged at two or more sheet pectinate form, respectively. Furthermore, it becomes possible by setting up the distance from a cathode 2 to a screen 8 for a long time compared with a level and vertical deflection inter-electrode distance to make an electron beam irradiate on a screen 8 in the small amount of deviations. Consequently, level and a perpendicular can make deflection distortion small.
[0010] The screen 8 is constituted by applying a fluorescent substance 20 to the rear face of a glass plate 21 in the shape of a stripe. Moreover, the metal back and carbon (not shown) are also applied to the rear face of a glass plate 21. By deflecting horizontally the electron beam which passes one through tube 14 of the signal modulating electrode 4, the fluorescent substance 20 is constituted so that the fluorescent substance pair of three colors of R, G, and B can be irradiated by two trios, and it is perpendicularly applied in the shape of a stripe. In drawing 2 , the broken line on a screen 8 shows the partition of the perpendicularly it is displayed corresponding to each of two or more cathodes 2, and the two-dot chain line shows the horizontal partition displayed corresponding to each of the signal modulating electrode 4 of two or more sheets. The enlarged drawing of one partition lined [the broken line and] off into drawing 3 is shown.
[0011] it is shown in drawing 3 — as — one partition — a horizontal direction — if — the fluorescent substances R1, G1, and B1 of R, G, and B for two trios and fluorescent substances R2 and G2, and B-2 — having — a perpendicular direction — if — it has the width of face for eight lines. It is horizontal, and 1mm, the magnitude of 1 partition in this configuration is perpendicular, and is 3mm. In addition, in drawing 3 , although the fluorescent substance of R, G, and B which are three colors respectively is illustrated in the shape of a stripe, it may be arranged in the shape of a delta. However, when it has arranged in the shape of a delta, it is necessary to impress the horizontal deflection wave and vertical deflection wave which suited it. Moreover, in drawing 3 , it differs from the image which the proportion in every direction displayed on the actual screen on account of explanation. Moreover, in this configuration, although the fluorescent substance of R, G, and B is prepared by two trios to one through tube 14 of the signal modulating electrode 4, you may prepare above by a part for one trio, and 3 trios. However, it is necessary to add R of one trio or three trios or more, G, and B video signal to the signal modulating electrode 4 one by one, and to perform horizontal deflection in this case, synchronizing with it.
[0012] Below, the drive circuit of this image display device is shown in drawing 4 . First, the drive part for irradiating and displaying an electron beam on a screen 8 is explained. A power circuit 22 is a circuit for impressing predetermined bias voltage to each electrode of an image display device, and the direct current voltage of V8 is impressed to a back plate 1 on V5 and a screen 8 at V1 and the electron beam drawer electrode 3 at V3 and a focusing electrode 5, respectively.
[0013] A pulse generating circuit 39 is a circuit for creating a cathode driving pulse using

Horizontal Synchronizing signal H and Vertical Synchronizing signal V. The timing chart is shown in drawing 5 . As shown to I of drawing 4 - Ma, as for each cathodes 2I-2Ma, a heating condition is held so that a current may flow, and may be heated and a driving pulse (I - Ma) may emit an electron to the period whose driving pulse (I - Ma) is H level at the period which is L level. Thereby, an electron is emitted only for 8 horizontal-scanning period when the driving pulse (I - Ma) of low voltage is impressed, respectively from 28 cathodes 2I-2Ma. In order to constitute one screen, upper cathode 2 I to cathode 2 downward Ma should just change 8 horizontal-scanning period [every] level one by one.

[0014] Below, deviation actuation is explained. As shown in drawing 4 , the deflecting voltage generating circuit 40 is constituted by Direct-Memory-Access controller (henceforth DMA controller) 41, memory 42 for deflecting voltage wave storage (henceforth deviation memory), 43h [of digital to analog converters for horizontal deflection] (henceforth D/A converter for horizontal deflection), D/A-converter43v for vertical deflection, and 8BIT data latch 44h for horizontal deflection, and 8BIT data latch 44for vertical deflection v, and high-voltage amplifier 45h for horizontal deflection, and high-voltage amplifier 45for vertical deflection v etc. This deflecting voltage generating circuit 40 generates the horizontal deflection signal h, h' and the vertical deflection signal v, and v'. In this configuration, about the vertical deflection signal, it is set up so that it may indicate by the 224 horizontal-scanning period in consideration of an overscan in the 1 field. Moreover, the memory address area which has memorized the vertical deflection positional information corresponding to each Rhine is divided into the 1st field and the 2nd field which have 1 set of memory space, respectively.

[0015] In case it displays, data are read from the corresponding deviation memory 42, vertical deflection data are latched by 8 bit-data latch 44v for vertical deflection, it changes into an analog signal by D/A-converter 43v for vertical deflection, and the signal amplified by high-voltage amplifier 45v for vertical deflection is impressed to the vertical deflection electrode 7. The vertical deflection positional information memorized by the deviation memory 42 consists of data which are mostly regular for every 8 horizontal-scanning period, and although the wave changed into the deviation signal also serves as about 12 steps of vertical deflection signals, since it has the memory space for the 2 fields as mentioned above, it can tune a location finely for every horizontal scanning line.

[0016] Moreover, since the horizontal direction of an image display device is divided into plurality to a horizontal deflection signal, the deviation memory 42 has six data for every 1 horizontal-scanning period so that a deviation location can be finely tuned for every horizontal scanning with the need of making six steps carrying out horizontal deflection of the electron beam to a 1 horizontal-scanning period. Therefore, 448x6=2688 byte memory is required for 1 inter-frame noting that it indicates by the 448 horizontal-scanning period, but since the data of the 1st field and the 2nd field are shared, 1344 bytes of memory is used in fact. In case it displays, the deviation information corresponding to each horizontal scanning Rhine is read from the deviation memory 42, horizontal deflection data are latched by 8BIT data latch 44h for horizontal deflection, it changes into an analog signal by 43h of D/A converters for horizontal deflection, and the signal amplified by high-voltage amplifier 45h for horizontal deflection is impressed to a horizontal deflection electrode 6.

[0017] It is as follows when the above actuation is summarized. That is, with the electron beam drawer electrode 3, the electron beam emitted from the cathode with which the driving pulse of L level of the cathodes 2I-2Ma is impressed to the display period except the vertical-retrace-line period of the perpendicular periods is horizontally divided into 114 partitions, and constitutes 114 electron beam trains. After the through put of a beam is controlled by the signal modulating electrode 4 for every partition and this electron beam converges with a focusing electrode 5, as shown in drawing 5 A level display period is irradiated one by one every [6 / 1/] by a horizontal deflection electrode 18, 18', etc. to which the horizontal deflection signal h of the pair which changes to about six steps, and h' were impressed at the fluorescent substances R1, G1, and B1 of a screen 8 and fluorescent substances R2 and G2, B-2, etc. at each level display period. Thus, a color picture is displayed on a screen 8 by modulating an electron beam with a video signal for every 114 partitions, and irradiating fluorescent substances R1, G1, and B1 and

fluorescent substances R2 and G2, and B-2.

[0018] the next — modulation control action ****** explanation of an electron beam — it carries out. First, in drawing 4 , each video signal of R, G, and B inputted from the signal input terminals 23R, 23G, and 23B is impressed to 114 sets of sample hold circuit groups 31a-31n. Each sample hold circuit groups 31a-31n are constituted by six sample hold circuits corresponding to fluorescent substances R1, G1, and B1 and fluorescent substances R2 and G2, and B-2, respectively. The sampling pulse generating circuit 34 makes the level display period (about 50microsec) of the level periods (63.5microsec) carry out sequential generating of the 684 sampling pulses (114x6) Ra1-Rn2 corresponding to each sample hold circuit of 114 sets of sample hold circuit groups 31a-31n. 684 sampling pulses Ra1-Rn2 are impressed at a time to 114 sets of six sample hold circuit groups 31a-31n, respectively. By this in each sample hold circuit group The video signals SR1, SG1, SB1, SR2, SG2, and SB2 corresponding to the fluorescent substances R1, G1, B1, R2, and G2 for 2 picture elements of each partition when classifying one line into 114 pieces and B-2 are sampled and held according to an individual, respectively. 114 sets of video signals SR1, SG1, SB1, SR2, SG2, and SB2 by which sample hold was carried out are transmitted to 114 sets of memory 32a-32n all at once by the transfer pulse t after the sample hold termination for one line, and 1 horizontal-scanning period maintenance of the degree is carried out here. These held video signals SR1, SG1, SB1, SR2, SG2, and SB2 are impressed to 114 switching circuits 35a-35n.

[0019] Switching circuits 35a-35n are circuits which have the common output terminal which changes the individual input terminal of video signals SR1, SG1, SB1, SR2, SG2, and SB2, and them one by one, and outputs them, respectively, are changed to coincidence and controlled by the switching pulses r1, g1, b1, r2, g2, and b2 impressed from the switching pulse generating circuit 36. the switching pulses r1, g1, b1, r2, g2, and b2 — each level display period — 6 — dividing — a level display period — switching circuits 35a-35n are changed every [6 / 1/], time sharing of each video signals SR1, SG1, SB1, SR2, SG2, and SB2 is carried out, a sequential output is carried out and the Pulse-Density-Modulation (PWM) circuits 37a-37n are supplied. An each switching circuits [35a-35n] output is impressed to 114 sets of PWM circuits 37a-37n, and according to the magnitude of each video signals SR1, SG1, SB1, SR2, SG2, and SB2, Pulse Density Modulation of it is carried out, and it is outputted.

[0020] Below, drawing 6 is used and Pulse Density Modulation (PWM) is explained to a detail. As shown in drawing 6 , a counter 53 counts up using the clock generated in the reference clock generating section 50, a comparator 54 compares the output and digital image input which are counted-up 8 bits, and the standup location of an PWM wave in the PWM section 55 is determined. Moreover, the falling location of an PWM wave in PWM55 is determined by the reset signal, and an PWM output is obtained.

[0021] When the gradation nature of the image display by PWM has a fixed PWM period, it is decided by the frequency of the clock generated in the reference clock generating section 50, and gradation nature also becomes high, so that a frequency is high. The output of 114 sets of PWM circuits 37a-37n is impressed to 114 electric conduction plates 15 of the signal modulating electrode 4 of an image display device according to an individual as a signal for modulating an electron beam, respectively.

[0022] Below, the timing of horizontal deflection and a display is explained. The synchronousr control of switching circuits 35a-35n and the 43h of the D/A converters for horizontal deflection is carried out so that the change timing of the video signals SR1, SG1, SB1, SR2, SG2, and SB2 in switching circuits 35a-35n, and the fluorescent substances R1, G1, B1, R2, and G2 by 43h of D/A converters for horizontal deflection and the change timing of the horizontal deflection of the electron beam to B-2 may be in agreement, respectively. Thereby, when the electron beam is irradiated by the fluorescent substance R1, the exposure of the electron beam is controlled by the modulating signal corresponding to a fluorescent substance R1. It will be similarly controlled about the electron beam which irradiates fluorescent substances G1, B1, R2, and G2 and B-2, and the fluorescent substances R1, G1, B1, R2, and G2 of each picture element and luminescence of B-2 will be controlled by video signals SR1, SG1, SB1, SR2, SG2, and SB2, respectively. Thus, according to the video signal of an input, a luminescence indication of each

picture element is given. This control is performed by the 114-set (two every picture elements each) part coincidence for one line, one-line the image of 228 picture elements is displayed, sequential execution is carried out from upper Rhine about Rhine of the 224 further 1 fields, and an image is displayed on a screen 8. Furthermore, many above-mentioned actuation is repeated for every field of an input video signal, and a television signal etc. is displayed on a screen 8.
[0023]
[Problem(s) to be Solved by the Invention] However, an PWM period needs to become short as horizontal scan frequency becomes high, and it is necessary to make the frequency of the clock for PWM high with the above configurations. Since the working speed of a semiconductor device becomes quick on the other hand so that the frequency of the clock for PWM becomes high, it becomes disadvantageous in respect of cost and power consumption. For this reason, there is a limitation in raising the frequency of the clock for PWM and raising gradation nature.
[0024] This invention aims at offering the image display device which can obtain the good high image of gradation nature, without raising the frequency of the clock for PWM, even if an PWM period becomes short as it is made in order to solve the above technical problems in the conventional technique, and horizontal scan frequency becomes high.
[0025]
[Means for Solving the Problem] The image display device concerning this invention is an image display device which performs a gradation display by the Pulse Density Modulation to which the width of face of the pulse for a display in each period which divides the horizontal scanning period of a video signal and is acquired is changed according to the magnitude of a video signal. A means to generate two or more clocks with which phases differ, and a clock selection means to choose one clock from two or more clocks according to a video-signal input, It is characterized by having a means to change the standup location of a Pulse-Density-Modulation output signal, based on the selected clock.
[0026] Preferably, a clock selection means chooses one clock from two or more clocks according to the lower bit of a digital video-signal input, and a means change the standup location of a Pulse-Density-Modulation output signal contains the comparator which compares with the high order bit of the output of a counter, and a digital video-signal input the counter which counts the selected clock, and the PWM section which determines the standup location of a Pulse-Density-Modulation output signal based on the output of a comparator.
[0027] According to the above configurations, gradation nature can be raised using the phase contrast of two or more clocks. Thereby, gradation nature can be raised, without raising the frequency of the clock for PWM. Consequently, it is not necessary to use the semiconductor device of high performance, and components cost can be reduced. Moreover, since it is not necessary to raise the clock frequency of a semi-conductor, it can contribute also to reduction of power consumption.
[0028]
[Embodiment of the Invention] Hereafter, this invention is explained still more concretely using the gestalt of operation.
(Operation gestalt 1) Drawing 1 is the block diagram showing the pulse-width-modulation (PWM) circuit of the image display device concerning the 1st operation gestalt of this invention. In drawing 1 , the reference clock generating section 60 generates the clock used as the criteria of PWM. The clock delay section 61 generates four clock a-d from which a phase differs from a reference clock. The clock selector 62 chooses and outputs one clock out of four clock a-d according to the condition of 2 bits of low order of a digital video signal. A counter 63 counts the selected clock and outputs the signal used as the criteria which determine the pulse width of PWM.
[0029] A comparator 64 compares the output and digital video signal of a counter 63, and outputs a comparison result. The PWM section 65 determines the standup location of an PWM wave based on the output of a comparator 64. A falling location is decided based on a reset pulse input, and is a fixed position. Thus, the pulse width of the PWM pulse outputted from the PWM section 65 changes by starting and changing a location. About the detail of this actuation, it mentions later. In addition, in drawing 1 , 66 shows the wave of four clock a-d from which the

phase outputted from the clock delay section differs, and 67 shows the wave of PWM output I corresponding to the selected clock - NI.

[0030] By matrix drive, the period of PWM becomes short according to ON or it being off, displaying an image and changing [of each pixel (picture element)] the die length of ON time amount (PWM), i.e., Pulse Density Modulation, so that the horizontal scanning period of a video signal becomes short in the image display device which indicates the brightness of each pixel by gradation, and the frequency of the clock for PWM for a gradation (for example, 256 gradation) display becomes high. In the case of the image display device using the PWM circuit by the conventional configuration especially shown in drawing 6 , since it is necessary to use the semi-conductor of high performance, the increment in cost or power consumption becomes large.

[0031] on the other hand, the clock generated in the reference clock generating section 60 in the image display device of this operation gestalt — being based — the clock delay section 61 -- drawing 1 — a wave — as shown in 66, the clock which is four kinds from which the phase shifted by a unit of 90 degrees is generated. Although it is four kinds in this example, three kinds of clocks shifted by a unit of 120 degrees may be used, and five or more kinds of clock ** of reverse finer phase contrast may be generated. Moreover, it is not necessary to necessarily carry out phase contrast of two or more clocks at equal intervals.

[0032] According to 2 bits of the low order of a digital video-signal input, the clock selector 62 chooses one clock from the above-mentioned clocks of four kinds of inside, and gives it to the counter 63 which determines the standup location of an PWM wave. A counter 63 counts this selected clock and counted value is given to a comparator 64 as a 6-bit output.

[0033] A comparator 64 measures data of 6 bits of high orders of a digital video-signal input, and the 6-bit output of a counter 63, and outputs a comparison result to the PWM section 65. The PWM section 65 determines the standup location of the PWM signal to output based on the output of a comparator 64. Moreover, about a falling location, it becomes the fixed position decided based on the reset pulse input f. Consequently, either of four kinds of PWM signals e (I - NI) as shown in drawing 1 by wave drawing 67 will be outputted from the PWM section 65. Four kinds of output waves of I - NI support four kinds of clock a-d chosen by the clock selector 62.

[0034] According to the above actuation, when an PWM period and display gradation (for example, 256 gradation) are the same, the value of the counter which determines the standup location of an PWM wave is good at 64 (6 bits) with this operation gestalt compared with 256 (8 bits) of the counter of the conventional PWM circuit (refer to drawing 6). That is, counted value becomes a quadrant. Therefore, when an PWM period is the same, the clock frequency of the counter which determines the standup location of an PWM wave also becomes a quadrant. Consequently, the semi-conductor of high performance is not needed but reduction of large cost and power consumption is attained compared with the conventional PWM circuit. On the contrary, when the same PWM clock frequency is used, 4 times [over the past] as many gradation nature as this can be obtained.

[0035]

[Effect of the Invention] As explained above, according to this invention, gradation nature can be raised by deciding the standup location of an PWM wave using two or more clocks with which phases differ, without raising the frequency of the clock for PWM. Consequently, the image of high quality can be displayed, without increasing cost and power consumption.

[Translation done.]